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Implementation of Energy Efficient Approximate Multiplier using 4-2 Compressor for Images

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Abstract—**Approximate computing is tentatively applied in some digital signal processing applications which have an inherent tolerance for erroneous computing results. The approximate arithmetic blocks are utilized in them to improve the electrical performance of these circuits. Multiplier is one of the fundamental units in computer arithmetic blocks. Moreover, the 4-2 compressors are widely employed in the parallel multipliers to accelerate the compression process of partial products. Meanwhile, an error- correcting module (ECM) is presented to promote the error performance of approximate multiplier with the proposed 4-2 compressors. The number of the approximate 4-2 compressor's outputs is innovatively reduced to one, which brings further improvements in the energy and area efficiency.**

I. INTRODUCTION :

In applications like multimedia signal processing and data mining which can tolerate error, exact computing units are not always necessary. They can be replaced with their approximate counterparts. Research on approximate comput

ing for error tolerant applications is on the rise. Adders and multipliers

form the key components in these applications. In approximate full adders.

Approximation techniques in multipliers focus on accumulation of partial products, which is crucial in terms of power consumption. Broken array multiplier is implemented, where the least significant bits of inputs are truncated, while forming partial products to reduce hardware complexity. The proposed multiplier saves few adder circuits in partial product accumulation. Two designs of approximate 4-2 compressors are presented and used in partial product reduction tree of four variants of 8 × 8 Array multiplier.

The major drawback of the proposed compressors is that they give nonzero output for zero valued inputs, which largely affects the mean relative error . The approximate design proposed in this brief overcomes the existing drawback. This leads to better precision. In static segment multiplier proposed, m-bit segments are derived from n-bit operands based on

leading 1 bit of the operands. This leads to better precision. In static segment multiplier (SSM) proposed, m-bit segments are derived from n-bit operands operands.

II. LITERATURE SURVEY :

H.R. Madiani, A.Ahmadi, S.M.Fahraie, and C. Lucas , proposed a defined

method on method on "**Bio-Sphere imprecise computational blocks for efficient VLSI implementation of soft-computing applications**" in this system conventional digital hardware computational blocks with different structures are designed to compute the precise results of the assigned calculations. The main contribution of our proposed Bio-inspired Imprecise Computational blocks is that they are designed to provide an applicable estimation of the result instead of its precise value at a lower cost. hardware defuzzification block of a fuzzy processor.

Jiangmin Gu And chip-hong chang , proposed a method on "**Low voltage, low power (5:2) compressor cell forfast arithmetic circuits"**, in this paper presents a new (5:2) compressor circuit capable of operating at ultra-low voltages. Its power efficacy is derived from the novel design of composite XOR- XNOR gate at transistor level. The new circuit eliminates the weak logic and threshold voltage drop problems, which are the main factors limiting the performance of pass transistor based circuits at low supply voltages.

Chip-hong chang, senior member, IEEE, Jiangmin gu, studentmember, IEEE, and mingyan zhang, student member, IEEE , proposed a method of "**Ultra low voltage low power CMOS 4-2 and 5-2 compressor for fast arithmetic circuits"** in this paper presents several architectures and designs of low-power 4-2 and 5-2 compressors capable of operating at ultra low supply voltages. These compressor architectures are anatomized into their constituent modules and different static logic styles based on the same deep sub micrometer CMOS process model are used to realize them. Different configurations of each architecture, which include a number of novel 4-2 and 5-2 compressor designs, are prototyped and simulated to evaluate their performance in speed, power dissipation and power-delay product.

R.Ramkumar, V.Sreedeep and Harish M kittur proposed a method of **"A design technique for faster array multiplier",** in this work faster column compression multiplication has been achieved by using a combination of two design techniques: partition of the partial products into two parts forindependent

parallel column compression and

acceleration of the final addition using a hybrid adder proposed in this work. Based on the proposed techniques 8, 16, 32 and 64- bit Array Multiplierare developed and compared with the regular Array . III. EXISTING SYSTEM :

In Existing Design, two designs of approximate 4-2 compressors are presented and used in partial product reduction tree of four variants of 8 × 8 Array multiplier. The major drawback of the proposed compressors is that they give nonzero output for zero valued inputs, which largely affects the mean relative error. Four different schemes for utilizing the proposed approximate compressors are proposed and analyzed for a Array multiplier. Extensive simulation results are provided and an application of the approximate multipliers to image processing is presented.

1.) EXISTING SYSTEM TECHNIQUE:

Array Multiplier design based on approximate 4-2 compressors. But it has some several drawbacks. In this multiplier, for an n-bit input, the right most columns of partial product matrix is completely truncated and the approximate compressors are used from (n2 + 1) th column to column.

2.) EXISTING SYSTEM DRAWBACKS:

i.) More Error
ii.) Complicated to implement in Practical Time
iii.) More Complexity in Logic SimplificationIV .PROPOSED SYSTEM :

This paper purposed Edge Detection using Sobel Operator in Digital Image Processing and and implementation using Verilog HDL. Firstly, a jpg image is inputted and converted into binary image with the help of MATLAB. Acquire a jpg image, which is by default in an RGB color space and convert this RGB image to grey level image. Now convert the grey level image into the binary image. This binary image is very large, so it is resized and written into a text file

. Further implementation is done on the Xilinx ISE and Modelsim . The Sobel operator is used commonly in edge detection its based on proposed multipliers. At each point in the image, the result of the Sobel operator is the corresponding norm of this gradient vector. Modeslim read the text file generated by the MATLAB into the memory and store it into the RAM, then extract the Image window.

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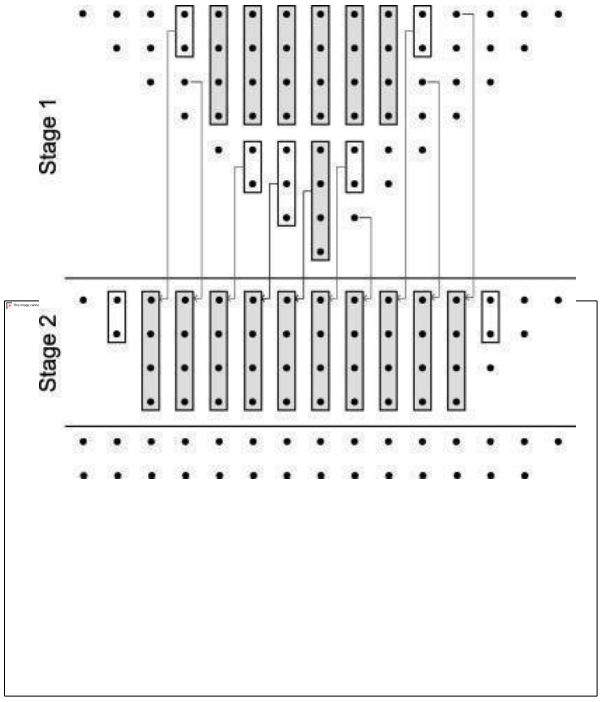
1.) PROPOSED SYSTEM TECHNIQUE:



These approximate compressor based Multiplier for Sobel Edge Detection Application.Three approximate 4-2 compressors (UCAC1, UCAC2, and UCAC3) are proposed in this section. Then, the ECM is presented to detect an input pattern with a large probability and correct the erroneous compensation in this case. Furthermore, the proposed designs are embedded in 8-bit multipliers based on the partial product tree. And all the analyses are performed with the uniform distribution.

2.) PROPOSED MULTIPLIER BLOCK DIAGRAM:

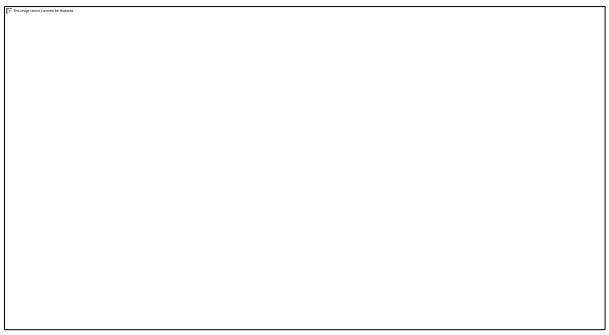
Array Multiplier

This figure shows the block diagram of array multiplier ,where digitalcombinational circuit used for multiplying two binary numbers.

Dadda Multiplier

The figure shows dadda multiplier , which is a hardware binary multiplier design and has same number of reduction stages as Wallace multiplier

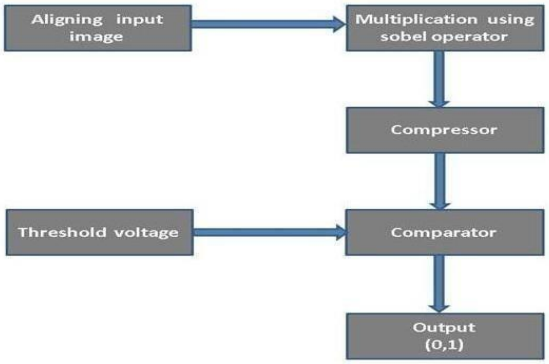
3.) PROPOSED SYSTEM FOR SOBEL EDGE DETECTION BLOCK DIAGRAM



The block diagram depicts the steps for performing sobel edge detection . The first step is to load any image and resize the image , and convert RGB to gray conversion , after that convert into binary number and we perform sobel operator .Thus we get output

image
at last step.

Flow Chart



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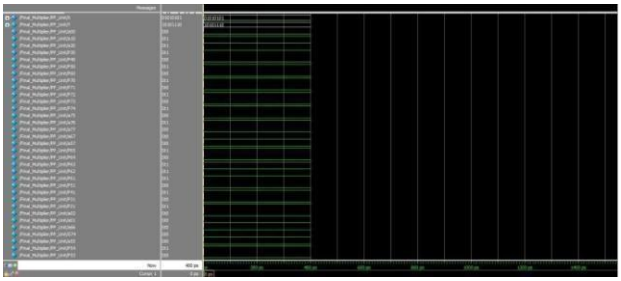
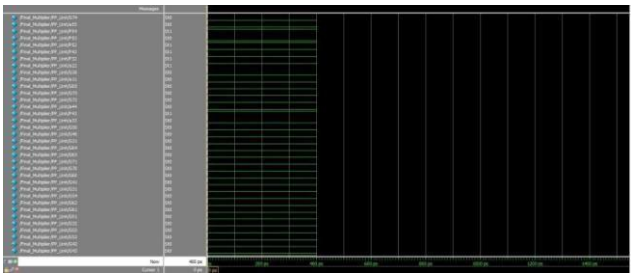
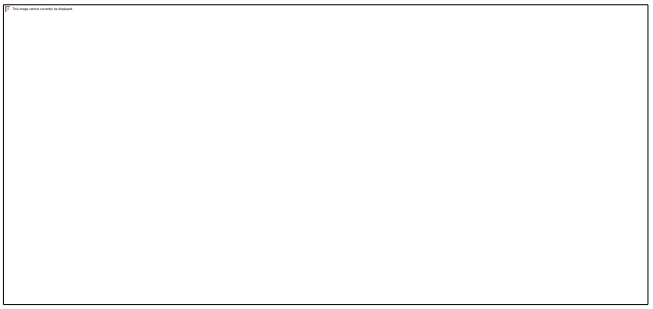
V. RESULTS

PARTIAL PRODUCT GENERATION BLOCK

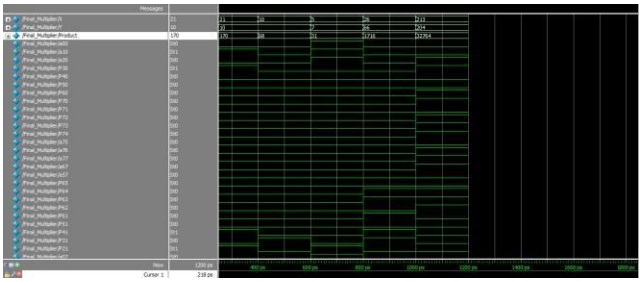




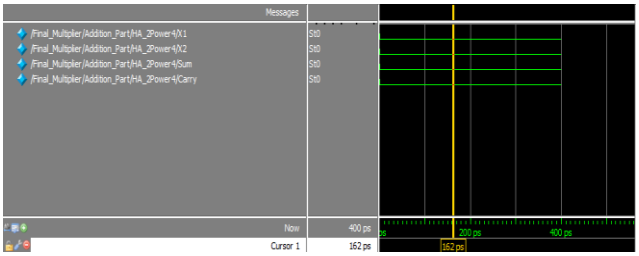
APPROXIMATE 4-2 COMPRESSOR

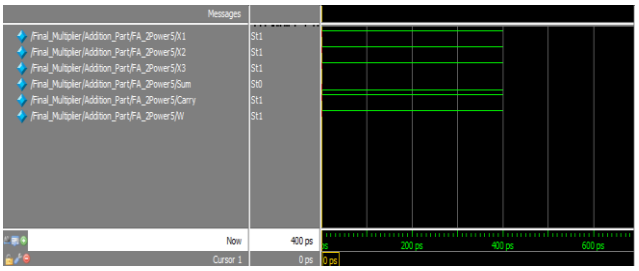


FINAL MULTIPLIER



APPROXIMATE HALF AND FULLADDER





NORMAL MULTIPLIER MAC DESIGN

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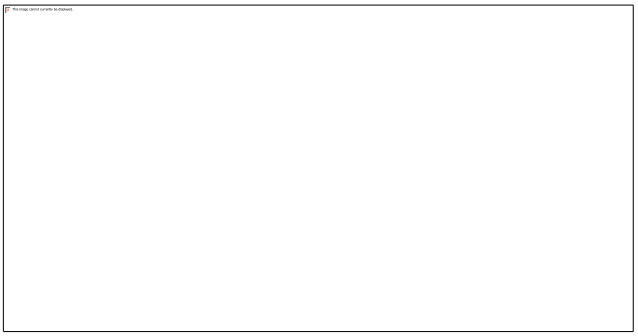
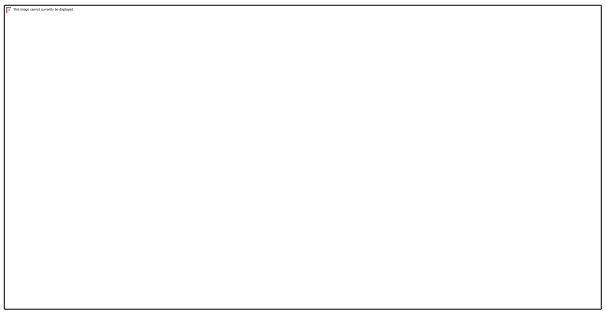
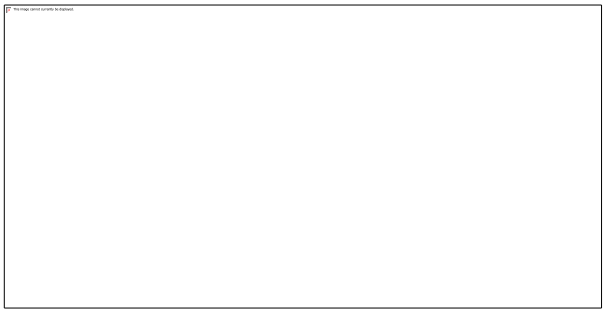
RTL ADDER PART

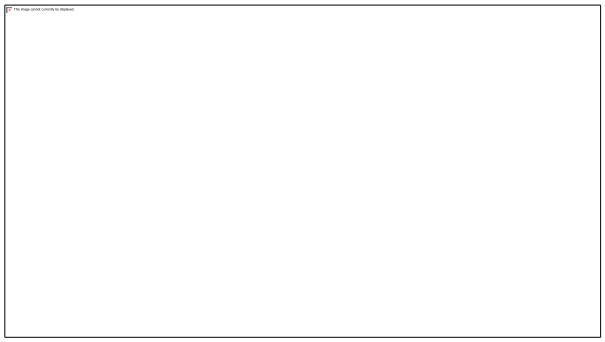
TECHNOLOGY DIAGRAM

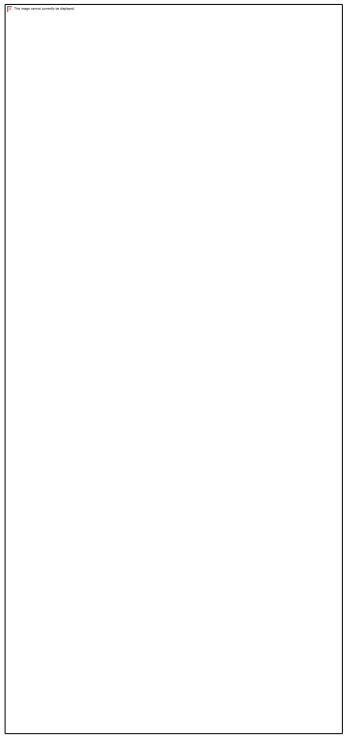


RLT SCHEMATIC









VI.) CONCLUSION :

All approximate multipliers are designed for n = 8. The multipliers are implemented in Verilog and synthesized using this paper deals with the analysis and design of two new approximate 4-2 compressors for utilization in a multiplier. we will design a Efficient Array Multiplier using our proposed Multiplier. The proposed approximate compressors are proposed and analyzed for a Array multiplier. This Proposed Multiplier is used in sobel operator design. Sobel operator executed in matlab and modals software. The Proposed method is implemented using Verilog HDL and Simulated and Synthesised by modelsim and Xilinx tools. The Design was analysed by Xilinx Tool.

VII. REFERENCES :

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